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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,470	12/27/2001	Derek Tam	1875.1350000	7771

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 08/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,470	TAM ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohwa (6,303,957 B1) in view of Tarabbia et al. (6,351,020 B1, hereinafter "Tarabbia").

Regarding Claims 1 and 16:

Ohwa discloses (in Fig. ***21*** and col. 11, line 48 to col. 12, line 18) a semiconductor device (and method of making the device) comprising:

an N-type substrate 204;

a P-type region 208 within the N-type substrate;

a thick oxide 218 formed over said P-type region;

a gate electrode 222 formed over said thick oxide and coupled to a first voltage supply line; and

P^+ pick-up terminals (214, 216) within said P-type region adjacent the gate electrode and coupled to a second voltage supply line; and

whereby said semiconductor device functions as a capacitor during operations.

Ohwa **lacks** the gate electrode being doped P^+. Tarabbia **teaches** a MOS capacitor structure, similar to that disclosed by Ohwa, formed with both an N-type ***capacitor*** and P-type ***capacitor such that a "cumulative" capacitor is acquired. Tarabbia teaches (in col. 6, lines 4-32) that a "cumulative" capacitor having such a structure provides improved control over the linearity characteristics of a capacitor integrated into semiconductor devices formed by CMOS fabrication processes***. In column 4 (lines 4-7), Tarabbia discloses the impurity type for the top plate depends on whether a P-type or an N-type capacitor is being formed***, i.e., the top plate of the p-type capacitor is heavily doped with a p-type impurity and the top plate of the n-type capacitor is heavily doped with an n-type impurity (note col. 3, lines 30-32).*** (Note: the top plate would be the gate electrode within the MOS capacitor). It would have been obvious to one of ordinary skill in the art to modify Ohwa by forming a P^+ gate electrode because Tarabbia teaches ***that a MOS capacitor structure having an N-type capacitor and a P-type capacitor would provide a "cumulative" capacitor structure that allows'improved control over its linearity characteristics.***

Regarding Claim 2:

This claim contains a limitation for some specific application/use of the device of Claim 1. Since Ohwa (in view of Tarabbia) discloses the device of Claim 1, it would have been

obvious to one of ordinary skill in the art to modify Ohwa (in view of Tarabbia) by specifically reciting a gate-to-substrate voltage because the device would be utilized according to design needs, i.e., one could have easily specified a gate-to-substrate voltage equal to zero volts, or greater than zero volts, or slightly greater than zero volts, etc., wherein a specific voltage would depend on a particular design/application.

Regarding Claims 3-5 and 17-19:

Ohwa discloses the gate comprises polysilicon (col. 12, lines 5-6); the N-type substrate 204 comprises a deep well (Fig. 21 and col. 11, lines 53-61); and the gate oxide typically having a thickness of 50-200 Å (col. 10, lines 24-25).

4. Claims 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohwa (6,303,957 B1) in view of Tarabbia (6,351,020 B1), Applicant admitted prior art (hereinafter "APA"), and Kriedt et al. (4,335,359, hereinafter, "Kriedt").

Regarding Claims 6 and 11:

These claims contain limitations for specifically integrating the capacitor of Claims 1-5 into a low-pass filter, wherein the low-pass filter is part of a phase locked loop (PLL) circuit. Note Ohwa (in view of Tarabbia) discloses all limitations of the capacitor. Furthermore, note that APA discloses (in Fig. 1 and pages 1-4) all elements of the PLL circuit specified in Claim 6, excluding the specific structure of the capacitor integrated into the low-pass filter. Kriedt is **cited only to show** it was very well known at the time the current invention was made to integrate a MOS capacitor into a low-pass filter circuit (note Kriedt, col. 2, lines 11-12). It would have been obvious to one of ordinary skill in the art to modify Ohwa (in view of Tarabbia)

by specifically incorporating the capacitor into a low-pass filter circuit and further integrating the low-pass filter into a PLL circuit because Kriedt shows it was well known in the art to incorporate a MOS capacitor into a low-pass filter and APA shows it was well known in the art that a PLL circuit would include a low-pass filter. In other words, one of ordinary skill would have found it obvious to specifically integrate the MOS capacitor of Ohwa (in view of Tarabbia) into any known circuitry such as the PLL circuit with a low-pass filter (as disclosed by APA), wherein the MOS capacitor could be specifically incorporated into the low-pass filter as shown by Kriedt.

Regarding Claims 7-10 and 12-15:

These claims are similar to Claims 2-5, which were specifically addressed above; therefore, they are held obvious over the cited references with reasoning similar to those applied to Claims 2-5 above.

Remarks

5. Applicants' remarks/arguments have been carefully reviewed and considered, but they are not persuasive. Applicants generally submit that Tarabbia does not teach or suggest that "the impurity type for the top plate depends on whether a P-type or an N-type capacitor is being formed". Tarabbia clearly discloses that the top plate "206" of the n-type capacitor is doped with n-type impurity, and unlike top plate "206" of the n-type capacitor, the top plate "406" of the p-type capacitor is doped with p-type impurity (note Tarabbia, col. 3, lines 30-32; and col. 4, lines 4-7). Applicants further submit that Tarabbia does not provide any motivation for the alleged combination. In response to Applicants' submission, specific portions of Taribbia's disclosure

are further cited in this Office action, in order to clearly show at least one reason why one of ordinary skill in the art would have been motivated to modify Ohwa by using "a P^+ gate electrode formed over...thick oxide". Therefore, Applicants' remarks/arguments are not persuasive and all pending claims (1-19) stand rejected under 35 USC § 103.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 703-306-5986.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Applicant should note that effective May 1, 2003, the United States Patent and Trademark Office has a new Commissioner for Patents address for transitioning to the new Office location in Alexandria, VA, wherein correspondence in patent-related matters to organizations reporting to the Commissioner for Patents must now be addressed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Lex Malsawma

July 29, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800